IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Michael Frank, Ricardo J. Motta, Justin Reyneri, David Xiao Dong Yang, William R. Bidermann, Odutola Oluseye Ewedemi		
Assignee:	Pixim, Inc.		
Title:	Video Imaging System Including a Digital Image Sensor and a Digital Signal Processor		
Serial No.:	10/634,302	Application Control No.:	7966
Examiner:	Nicholas G. Giles	Group Art Unit:	2622
Docket No.:	PIX-P-033	Filing Date:	August 4, 2003
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San Jose, California
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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 CFR § 41.37

Dear Sir:

Applicant submits this Appeal Brief pursuant to the Notice of Appeal filed in the present case on June 25, 2008. This brief is filed with on-line payment of $255.00, being the amount specified in 37 CFR 41.20(b)(2) for this Appeal Brief. The Commissioner is also authorized to deduct any other amounts required for this appeal brief and to credit any amounts overpaid to Deposit Account. No. 502226.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Pixim, Inc., as named in the caption above.

II. RELATED APPEALS AND INTERFERENCES

Based on information and belief, there are no appeals or interferences that could directly affect or be directly affected by or have a bearing on the decision by the Board of Patent Appeals in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-31 are pending in the case, of which claims 8-31 are withdrawn from consideration. Claims 1-7 are rejected. Specifically, in the Final Office Action dated March 25, 2008, the Examiner maintained his rejection of claims 1 and 7 under 35 U.S.C. §103(a) as being unpatentable over a combination of four references: Horii et al. (USP 6,573,931; hereinafter "Horii") in view of Yamada et al. (USP 5,995,137; hereinafter "Yamada") further in view of Fowler (USP 5,461,425) and in further view of Ewedemi et al. (U.S. Pat. Pub. No. 2001/0040631; herein after "Ewedemi"). The Examiner further maintained his rejection of claims 2-6 under §103(a) as being unpatentable over Horii in view of Yamada and further in view of Fowler and further in view of Ewedemi and further in view of Tamama et al. (U.S. Pat. Pub. No. 2002/0135683; hereinafter "Tamama").

The rejection of claims 1-7 is appealed. The pending claims are listed in the Claims Appendix below.

IV. STATUS OF AMENDMENTS

No claim amendments were made after the Final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed invention is directed to a video imaging system including a digital image sensor and a digital image processor. The digital image sensor is implemented as a digital pixel sensor for providing high quality images with enhanced dynamic range. The digital image processor implements signal processing functions, such as for generating video images in a number of video formats and for providing image enhancement functions. (Applicant's specification, paragraph [0034].)

In particular, the digital image sensor and the digital image processor communicates over a fully digital communication interface where pixel data are transferred from the digital image sensor to the digital image processor over a pixel bus and the control information are transferred between the digital image sensor and the digital image processor over a separate control interface bus. (Applicant's specification, paragraph [0041].)

A feature of the video imaging system of the claimed invention is that the digital image sensor performs image capture operations ***independent of*** the image processing operations performed by the digital image processor. Applicant's specification, paragraph [0036], recites: "The digital image sensor can be **operated autonomously**. That is, image capture is carried out by the digital image sensor **completely independently** of the digital image processor. The digital image sensor **delivers only complete image data** to the digital signal processor" (emphasis added). Applicant's specification, paragraph [0039], further explains:

> Digital image sensor 102 is an **operationally "stand-alone" imaging subsystem and is capable of capturing and recording image data independent of digital image processor 104**. Digital image sensor 102 operates to collect visual information in the form of light intensity values using an area image sensor, such as sensor array 210, which includes a two-dimensional array of light detecting elements, also called photodetectors. Sensor array 210 collects image data under the control of a data processor 214. **At a predefined frame rate, image data collected by sensor array 210 are read out of the photodetectors through readout circuit 211 and stored in an image buffer 212**. Typically, image buffer 212 includes enough memory space to store at least one frame of image data from sensor array 210. Digital image sensor 102 may further include a memory 215 for storing microcode instructions used by data processor 214. (Emphasis added.)

Applicant's specification further explains that "the digital image sensor of the video imaging system **does not receive timing information from the digital signal processor** but rather operates in response to a protocol for delivering full frame of image data on demand. Thus, the digital image sensor of the video imaging system **can operate autonomously during image capture and interacts with the digital image processor only for transferring a full frame of pixel data**" (paragraph [0089], emphasis added).

The claimed invention of claim 1 recites a video imaging system including a digital image sensor for performing image capture operations and a digital image processor for performing image processing operations. The digital image sensor includes a sensor array, an image buffer for storing the pixel data, a first processor and a first interface circuit. The digital image processor includes a second interface circuit, a frame buffer, an image processing pipeline and a second processor. The digital image sensor transfers pixel data onto a pixel bus to the digital image processor. The digital image sensor and the digital image processor transfer control information over a control interface bus separate from the pixel bus. Finally, the digital image sensor performs image capture operations independent of the image processing operations performed by the digital image processor.

Claims 2-7 are dependent claims of claim 1 and are directed to various features of the video imaging system.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 1-7 are unpatentable under 35 U.S.C. § 103(a) as being unpatentable over Horii, Yamada, Fowler, Ewedemi and Tamama.

VII. ARGUMENTS

Claims 1-7 are pending in the present application of which Claim 1 is the only independent claim. In the Final Office Action dated March 25, 2008, the Examiner maintains his rejection of claims 1-7 under 35 U.S.C. §103(a) because the Examiner contends that the combination of the four references, including modifications of the references thereof, discloses every limitation of the rejected claims. More specifically, the Examiner contends that Figure 7 and related descriptions of Horii describes substantially all limitations of claim 1 except for selecting from a group of video formats and a sensor array of digital pixels. The Examiner relies on Yamada and Fowler for reciting selecting different video formats and digital pixels. Furthermore, the Examiner contends that Horii, Yamada and Fowler are silent with regard to having separate control interface and pixel buses and the Examiner cites Ewedemi for disclosing a pixel data bus and a control bus. (See Final Office Action, pp.2-4.)

In the Advisory Action dated June 6, 2008, the Examiner admits that Horii does not disclose an image buffer in the camera unit but contends that data briefly passes through the multiplexor and demultiplexor units in the camera unit and therefore are temporarily

remembered (buffered). However, in the combination of Horii and Ewedemi, the multiplexor and demultiplexor units would have to be eliminated to allow the use of separate data and control buses. The Examiner then contends that the replacement of the multiplexing and demultiplexing unites with separate data buses still requires interface connections at the connection points of the busses which in turn would act as the image buffer since data briefly passes through. The Examiner also refers to memory 110 and memory interface port 22b of Ewedemi which can act as a buffer. (See Advisory Action, Continuation Sheet.)

Applicant submits that the rejections of the independent claims and the associated dependent claims are improper for the following reasons.

1. The Cited References

Horii describes in Fig 7 a video input apparatus where a zoom camera unit 150 is connected to a video processing unit 200 through a cable 109. The zoom camera unit 150 of Horii does not include any memory buffer for storing the pixel data. Instead, Horii states specifically that the "data multiplexing and demultiplexing unit 115 multiplexes the video signal 114 and control data from the system control unit 106, and transmits multiplexed data to the image processing unit 200" (Horii, col. 2, ln. 1-5). The data multiplexing and demultiplexing unit 115 does not act as an image buffer for ***storing*** pixel data because the data multiplexing and demultiplexing unit is used for combining video signal and data onto a single data stream. The ***goal*** of Horii is to ***multiplex*** the image data and the control data and ***transmit the multiplexed data*** on the same bus between the zoom camera unit and the video processing unit. Horii's system will not work if the multiplexing/demultiplexing units are removed.

Furthermore, Horii in col. 1, ln. 38-43, describes the operation of the system control unit 106 for providing two-way communications with the image processing unit (200) and interpreting commands from the host unit (400) to execute operations requested by the host unit. Horii further explains that "in order to realize auto-focusing and automatic exposure [in zoom camera unit], data required for such control must be read out from a signal processing circuit 202 [in video processing unit 200] and must be transmitted to a zoom camera unit 150." (Horii, col. 8, ln. 24-27.) In addition, Horii explains that:

> **The signal processing circuit** 202 [in the video processing unit] generates an interrupt signal and supplies it to a system control unit

> 250 so as **to inform the system control unit 250 of synchronization data** such as brightness data of the object used in exposure control, white balance data for white balance control, in-focus data for focusing control, and the like…**the system control unit 250** [in the video processing unit] **transmits synchronization data** such as the brightness data of the object for automatic exposure, in-focus data for focusing control, and the like **to the zoom camera unit 150** during the vertical blanking interval." (Horii, col. 8, ln. 28-40; emphasis added.)

Therefore, the zoom camera unit of Horii does not perform image capture operation independently but rather depend on the video processing unit to provide synchronization data, in-focus data and the like.

Ewedemi describes an image sensor including an integrated on-chip memory and a memory interface for outputting pixel data. By including a memory interface in the image sensor, the image sensor can be coupled directly to the memory interface port of an external image processing unit. The image processing unit is able to access the image sensor using conventional memory interface protocols. For example, the image sensor can support a SRAM, a DRAM or a RAMBUS memory interface. By providing an on-chip memory and a memory interface in an image sensor, the image sensor facilitates high speed pixel readout between the image sensor and the image processing device. The pixel data transmission bandwidth is limited only by the speed of the memory interface. Furthermore, by using the memory interface of the image sensor for sensor readout, the image processing device can access pixel data in the image sensor with greater convenience and flexibility not available in conventional image sensors.

To that end, Ewedemi describes with reference to Figure 2 an interface protocol conversion circuit 114 in the image sensor which communicates with the memory interface port 22b of the image processing unit. The image sensor communicates with image processing unit on a pixel data bus 115 and a control bus 116 using a memory interface protocol. Examples of memory interface protocols are DRAM interface protocol and a SRAM interface protocol.

2. Independent Claim 1 is patentable over the cited reference

Independent claim 1, reciting "said digital image sensor and said digital image processor transfer control information over a control interface bus coupled between said first

interface circuit and said second interface circuit and separate from said pixel bus" and "said digital image sensor performs said image capture operations independent of said image processing operations performed by said digital image processor" is patentable over the four cited references including Horii for at least the following reasons. First, Horii teaches away from using separate pixel bus and control interface bus as Horii specifically requires the use of video signal and control data multiplexing. Second, any attempts to modify Horii by removing the multiplexing/demultiplexing unit would destroy the entire functionality of Horii and would constitute impermissible hindsight resconstruction. The combination of the four references to meet the limitations of claim 1 would require wholesale redesign of Horii using Applicant's claimed invention as a template. Finally, any combination of the four references still does not teach or suggest "said digital image sensor performs said image capture operations independent of said image processing operations performed by said digital image processor," as recited in claim 1.

3. Horii teaches away from the claimed invention

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would **lead away** from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock*, Inc., 721 F.2d 1540, 1550 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984) (emphasis added). "It is not permissible to pick and choose only so much of any given reference as will support a given position and ignore the reference in its totality." *Lubrizol Corp. v. Exxon Corp.*, 696 F. Supp. 302, 7 USPQ2d 1513, 1527 (N.D. Ohio 1988), citing *Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc.*, 796 F.2d 443, 448 (Fed.Cir.1986), cert. denied 484 U.S. 823, 108 S. Ct. 85, 98 L. Ed. 2d 47 (1987). When Horii is viewed in its entirety, one of ordinary skill in the art would appreciate that Horii is directed to a video imaging system using multiplexing of the video signal and control data. The use of video signal/control data multiplexing is critical to the practice of the video imaging system of Horii.

Horii teaches away from the claimed invention of claim 1 by describing the use of the same bus to transmit pixel data and control information by use of multiplexing. To that end, Horii includes Multiplexing and Demultiplexing Unit 115 and 231 in respective zoom camera unit 150 and video processing unit 200 to realize the multiplexing and demultiplexing function. Claim 1 recites specifically that the pixel bus for transferring pixel data and the control interface bus for transferring control information are separate from each other and no

multiplexing is used. Therefore, by use of a multiplexing/demultiplexing unit, Horii teaches multiplexing of the video signal and the control information and thereby teaches away from using separate pixel and control interface buses. Horii thereby cannot be combined with other references, such as Ewedemi, where separate pixel data and control data buses are used.

In view of the requirement that the Examiner must read each references **as a whole**, including the portion of the reference that teach away from the claimed invention, Applicant submits that Horii should be removed as a reference altogether. Horii cannot be used in the combination suggested by the Examiner because that would require one to ignore portions of Horii that teaches away from the claimed invention which is prohibited by numerous case laws. ("A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would **lead away** from the claimed invention." *W.L. Gore & Associates, Inc. v. Garlock*, Inc., 721 F.2d 1540, 1550 (Fed. Cir. 1983); "It is not permissible to pick and choose only so much of any given reference as will support a given position and ignore the reference in its totality." *Lubrizol Corp. v. Exxon Corp.*, 696 F. Supp. 302, 7 USPQ2d 1513, 1527 (N.D. Ohio 1988).)

4. Examiner engages in impermissible hindsight reconstruction

In the §103(a) rejection of claim 1, the Examiner combined four references: Horii, Yamada, Fowler and Ewedemi to render claim 1 obvious. Applicant submits that the Examiner is engaging in **impermissible hindsight reconstruction** in arriving at the §103(a) rejection of claim 1. The Federal Circuit in *In re Fritch* states that:

> It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that "one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. *In re Fritch*, 972 F.2d 1260, 1266 (Fed. Cir. 1992).

Here, the Examiner relied on four different references for various isolated disclosure of the claim limitations of claim 1. There is no indication that the four references can be combined at all in the manner suggested by the Examiner, particularly when Horii and Ewedemi describe entirely different interface bus structures for the image sensor/image processor interface. More importantly, the combination suggested by the Examiner requires **wholesale**

redesign to be made to Horii which would completely destroy the functionality of the zoom camera unit and the video processing unit in Horii. This is because Horii relies on the video signal/control data multiplexing to transfer control information to and from the zoom camera unit. Ewedemi describes an image sensor and an image processing unit communicating with each other on a pixel data bus 115 and a control bus 116 ***using a memory interface protocol***. There is nothing in any of the references to suggest that Horii can be modified to incorporate the data bus structure and using a memory interface protocol as described in Ewedemi.

In the final office action and the advisory action, the Examiner first relied on Multiplexing and Demultiplexing Unit 115 to meet the limitation of the image buffer limitation of claim 1. The combination of Horii and Ewedemi would necessarily require the elimination of Multiplexing and Demultiplexing Unit 115 and therefore the combination will no longer meet the limitations of claim 1. The Examiner attempted to introduce an image buffer back into the Horii and Ewedemi combination by suggesting that an interface connection would be added when the Multiplexing and Demultiplexing Units are removed. However, such conclusion constitutes impermissible hindsight reconstruction as the Examiner is merely using the claimed invention as a template to piece together the prior art.

More specifically, in the Advisory Action, the Examiner acknowledges that the combination of Horii and Ewedemi would eliminate the Multiplexing and Demultiplexing Unit 115 and suggests that "the replacement of the multiplexing and demultiplexing unites with separate data buses still requires interface connections at the connection points of the busses which in turn would act as the image buffer since data briefly passes through." The assumption made by the Examiner is purely based on the claimed invention and the Examiner is merely using the claimed invention as a template. Where the combination of references obfuscates certain elements, the Examiner pulls the missing elements out of thin air.

Without Applicant's claimed invention as a template, one of ordinary skill in the art, looking at Horii, Ewedemi and the other cited references **would not be able to** take apart elements of the cited references and piece them together to form the claimed invention in the manner suggested by the Examiner. The combination suggested by the Examiner would require wholesale redesign of Horii and Ewedemi in accordance with the claimed invention which constitutes impermissible hindsight reconstruction.

5. Cited references do not teach all limitations

Any combination of Horii and Ewedemi and other references still does not teach or suggest all limitations of claim 1. Claim 1 recites "said digital image sensor performs said image capture operations ***independent*** of said image processing operations performed by said digital image processor." The Examiner relied on Horii for describing this limitation but in the relevant section of Horii referred to by the Examiner, Horii actually does not teach or suggest this limitation of claim 1. There is nothing in Horii that recites that the image capture operation is performed independently of the image processing operations. Horii merely describes the operation of the system control units 106 in the zoom camera unit where the zoom camera unit receives commands from the host unit and executes the commands. There is no description that the image capture operation is carried out by the zoom camera unit independently of the video processing unit.

Furthermore, as discussed above, the zoom camera unit requires control data, including synchronization data such as the brightness data of the object for automatic exposure, in-focus data for focusing control, and the like for the image capture operation and these control data are generated by the video processing unit and transmitted to the zoom camera unit during the vertical blanking interval. Therefore, the zoom camera unit in Horii in fact does not perform the image capture operation independently of the image processing operation but rather relies on the image processing operation for important synchronization data.

6. Claims 1-7 are patentable over the cited references

For the reasons stated above, claim 1 is patentable over the cited references. Claim 7, dependent upon claim 1, is patentable over the cited references at least for the same reasons claim 1 is patentable. Claims 2-6, dependent upon claim 1, are patentable over the Horii, Yamada, Fowler and Ewedemi at least for the same reasons claim 1 is patentable. Tamama does not cure the deficiency of Horii, Yamada, Fowler and Ewedemi. Claims 2-6 are therefore patentable over all of the cited references.

7. Rejoinder of Withdrawn Claims

Applicant submits that in the office action of February 28, 2007, Examiner indicated that claim 1 links inventions I to VI of claims 2-31 and Examiner states that claims 8-31 are eligible for rejoinder when claim 1 is indicated to be allowable. Claims 8-31 depend from

claim 1 and therefore include all the limitations of claim 1. For the reasons stated above, claim 1 is in condition for allowance. Therefore, rejoinder of claims 8-31 is respectfully requested. Claims 8-31, dependent upon claim 1, are patentable over the cited references at least for the same reasons claim 1 is patentable.

VIII. CONCLUSION

For the above reasons, Applicant respectfully submits that rejection of pending claims 1-7 is unfounded. Accordingly, Applicant requests that the rejection of claims 1-7 be reversed.

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/Carmen C Cook/	August 19, 2008
Attorney for Applicant(s)	Date of Signature

Respectfully submitted,

/Carmen C Cook/

Carmen C. Cook
Attorney for Applicant(s)
Reg. No. 42,433
Patent Law Group LLP
2635 N. First St.
Suite 223
San Jose, CA 95134
Tel (408) 382-0480 x208
Fax (408) 382-0481

CLAIMS APPENDIX

Claims on Appeal

1. (Previously Amended) A video imaging system, comprising:

a digital image sensor for performing image capture operations, comprising:

a sensor array comprising a two-dimensional array of digital pixels, each digital pixel outputting digital signals as pixel data representing an image of a scene;

an image buffer, in communication with said sensor array, for storing said pixel data;

a first processor, in communication with said image buffer and said sensor array, for controlling image capture and pixel data processing operations; and

a first interface circuit, in communication with said image buffer, for transferring said pixel data onto a pixel bus; and

a digital image processor for performing image processing operations, comprising:

a second interface circuit coupled to receive said pixel data from said pixel bus;

a frame buffer, in communication with said second interface circuit, coupled to store said pixel data;

an image processing pipeline for processing said pixel data stored in said frame buffer into video data corresponding to a video format selected from a group of video formats; and

a second processor, in communication with said frame buffer and said image processing pipeline, for directing said image processing pipeline to process said pixel data stored in said frame buffer;

wherein said digital image sensor and said digital image processor transfer control information over a control interface bus coupled between said first interface circuit and said second interface circuit and separate from said pixel bus and said digital image sensor performs said image capture operations independent of said image processing operations performed by said digital image processor.

2. (Original) The video imaging system of claim 1, wherein said image processing pipeline comprises an interpolator module, in communication with said frame buffer, for interpolating said pixel data to generate video data in at least three color planes and having a vertical resolution corresponding to said selected video format.

3. (Original) The video imaging system of claim 2, wherein said image processing pipeline further comprises an image processing circuit coupled to receive said video data from said interpolator module and for performing image enhancement functions on said video data.

4. (Original) The video imaging system of claim 2, wherein said interpolator module performs vertical interpolation and demosaic operations on said pixel data.

5. (Currently Amended) The video imaging system of claim 3 ~~claim 2~~, wherein said image processing circuit performs tone correction operations on said video data.

6. (Original) The video imaging system of claim 2, wherein said digital image processor further comprises a television encoder, in communication with said interpolator module, for encoding said video data in said selected video format and for providing control signals to said interpolator module for directing said interpolator module to process video data.

7. (Original) The video imaging system of claim 1, wherein said group of video formats comprises NTSC, PAL and digital TV video formats.

Claims 8-31 (Withdrawn).

EVIDENCE APPENDIX

NONE

RELATED PROCEEDINGS APPENDIX

NONE